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METHOD FOR MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT HAVING MULTILAYER WIRING STRUCTURE [SEKISO HAISEN KOZO WO MOTSU HANDOTAI SHUUSEKI KAIRO NO SEIZO HOHO]

Yasuhiro Maeda, et al.

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INVENTORS	(72):	MAEDA, YASUHIRO, ET AL.
APPLICANT	(71):	ADVANTEST CORP.

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METHOD FOR MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT HAVING MULTILAYER WIRING STRUCTURE

Specifications /1

Method for Manufacturing Semiconductor Integrated Circuit Having Multilayer Wiring Structure

Technical Field

This invention relates to a method for manufacturing a semiconductor integrated circuit having a multilayer wiring structure.

A highly integrated semiconductor integrated circuit is composed generally of a plurality of sub-circuits having various functions by stacking wiring layers forming basic elements.

Background Art

A semiconductor integrated circuit having a plurality of sub-circuits is shown in Figure 1. This semiconductor integrated circuit **A** has a plurality of sub-circuits **S1**, **S2**, ..., **Sk** (k=6 in the example if Figure 1). The sub-circuits can be large-scale functional blocks, such as a CPU, memory, DSP, AD converter and I/O interface, may be relatively small-scale or basic sub-circuits such as an adder, multiplier, multiplexer or flip-flop. Furthermore, the functional blocks and sub-circuits may be digital circuits, analog circuits or mixed signal circuits.

The semiconductor integrated circuit A has a multilayer wiring structure comprising a plurality of wiring layers (N-layers) as shown

* Number in the margin indicates pagination in the foreign text.

in Figure 2. A lowermost layer (1st wiring layer) provides a wiring connection between basic elements (transistors) formed on a semiconductor substrate, and is the wiring layer which constitutes a basic logic gate, which is a NAND gate or an inverter in the illustrated example, as shown in Figure 3. Input/output signal lines for the basic logic gates appear on the stacking surface of the 1st wiring layer. Shown within blocks of this drawing indicated by dotted lines are basic elements, which do not appear on the surface of the 1st wiring layer. The 2nd wiring layer provides a wiring connection between the basic logic gates formed from the 1st wiring layer, and is the wiring layer which constitutes relatively small scale sub-circuits, as shown in Figure 4, for example. Input/output signal lines for the sub-circuit appear on the surface of the 2nd wiring layer, but logic gates or inverters which constitute such circuits do not appear there. The i^{th} wiring layer ($3 \leq i \leq N-1$) is a wiring layer having sub-circuits formed up to the $(i-1)^{th}$ wiring layer wired and connected to each other and constitutes a larger-scale sub-circuit. The input/output signal line of the larger-scale sub-circuit appears on the multilayer face of th4e i^{th} wiring layer. The uppermost layer (N^{th} wiring layer) is a wiring layer having the sub-circuits (S1, S2, ..., Sk) formed of an $N-1^{th}$ wiring layer wired and connected to each other to constitute the semiconductor integrated circuit **A**. Only the input/output signal line of the semiconductor integrated circuit appears on the multilayer face of the N^{th} wiring layer, as shown in Figure 5. /2

The step for stacking each wiring layer is performed as shown in Figure 6. Firstly, although not shown in the drawing, a product from an immediately preceding step, namely, a substrate in which basic elements are formed, or an immediately preceding wiring layer is first deposited thereon of an oxide layer **11** such as formed by SiO_2, as shown in Figure 6(a). In a photolithography method, a mask is formed on the oxide layer **11** thereof for junctions with wirings or basic elements just below it, and then the reactive ion etching (RIE) technique is applied to form openings **12**, as shown in Figure 6(b). These openings **12** are filled with a conductive material, such as tungsten, to form junctions (stubs) **13**, as shown in Figure 6(c). As shown in Figure 6(d) next, an oxide layer **14** is formed by SiO_2 deposition. Photolithography is applied to the oxide layer **14** to define a mask and the reaction ion etching (RIE) technique is applied to form grooves **15** for regions to be wired, as shown in Figure 6(e). A layer **16** of a metal, such as Al, W or Cu, is formed, as shown in Figure 6(f), and the metal layer **16** is then subject to a chemical-mechanical polishing (CMP) to expose the oxide layer **14**. Wires **17** which fill the grooves **15** form a wiring **17** which is connected to the junctions **13** and also connected to the underlying wiring layer (not shown) through the junctions **13**. Steps to stack a wiring layer may follow a procedure shown in Figure 7. In a similar manner as illustrated in Figure 6, a condition as shown in Figure 7(a) is prepared in which junctions **13** fill in an oxide layer **11**. Subsequently, a metal layer **16** is formed over the entire surface,

as shown in Figure 7(b), and the application of the photolithography and the RIE technique form wires **17** connected to the junctions **13**, as shown in Figure 7(c). An oxide layer **18** is then deposited over the entire surface as shown in Figure 7(d), and the surface of the oxide layer **18** is planarized by CMP, as shown in Figure 7(e). In this case, when openings **12** are formed to provide the junctions **13**, the openings **12** should contiguously extend to reach the wires in the underlying wiring layer.

A method for manufacturing a semiconductor integrated circuit with a multilayer wiring structure has been briefly described above. In a conventional method for manufacturing a semiconductor integrated circuit, there has been no practice of testing basic elements or sub-circuits which have been already formed in the course of the manufacturing steps. /3

That is to say, a test of the semiconductor integrated circuit was performed by placing a probe in contact with bonding pads of a chip as shown in Figure 8 after the steps of manufacturing a semiconductor integrated circuit chip have been completed to provide an IC in a wafer state, inputting externally a test pattern to input pads on the circuit being tested, and observing a voltage response signal on a power supply pad of the circuit being tested or a current response signal through a power supply pad of the circuit being tested (wafer probing, die sort). Or, a test pattern is externally input into an input terminal (pin) of the circuit being tested, and a voltage response signal on an output terminal (pin) of the circuit being tested or a current response signal through a power supply terminal (pin) of the circuit being tested is observed to perform a test

of the semiconductor integrated circuit (package test or final test). Such tests will be hereafter referred to as final tests.

A stuck-at fault test, delay fault test, quiescent power supply current (I_{DDQ}, quiescent power supply current) test, functional test, exhaustive test, and the like also are performed as final test on the semiconductor integrated circuit. The stuck-at fault test is a method for observing the effect of a fault on a prescribed test pattern according to voltage signals through the output terminal of the circuit being tested, a fault in which a stuck-at fault is fixed at a certain constant value assuming stuck-at fault (a fault where the logic signal of the signal line is fixed at a certain constant value, a fault where a signal value is fixed at "0" is referred to as a stuck-at 0, and a fault where the signal value is fixed to "1" is referred to as a stuck-at 1) on a signal line in the circuit being tested. The delay fault test is a method for observing the affect of a fault on a prescribed test pattern array according to a voltage transition signal through the output terminal of the circuit being tested, assuming a delay fault in a signal propagating path or logic gate inside the circuit being tested, that is to say, a fault wherein the time required for a signal to propagate through a signal-propagating path or a logic gate (delay time) is larger or smaller than a prescribed value (the delay fault in the signal propagating path is called a path delay fault and the delay fault in the logic gate is called a gate delay fault). The quiescent power supply test is a method for observing the affect of a fault on a prescribed test pattern according to a quiescent

power supply current signal through the power supply terminal of the circuit being tested, assuming a short-circuit fault between a plurality of signal lines in the circuit being tested or a leakage fault in a basic element. The functional test is a method for test whether or not the function of the circuit being tested is operating correctly. The exhaustive test is a method for testing the output response of the circuit being tested with respect to a combination of all the signal values in the input terminal or the flip-flops of the circuit being tested. Moreover, a stuck-at fault test is described by, e.g. M. Abramovici, M.A. Breuer and A.D. Friedman (Digital Systems Testing and Testable Design, IEEE Press, New York, Chapters 6 and 8 (1990); a delay fault test is described by e.g., in G.L. Smith ("Model for Delay Faults Based upon Paths" Proceedings of IEEE International Test Conference (1985):342-349) and C.J. Lin and S.M. Reddy ("On Delay Fault Testing in Logic Circuits" Transactions on Computer-Aided Design CAD-6(5) (1987):694-703; a quiescent power supply current test is described by, e.g., S. Chakravarty and P.J. Thadikaran (Introduction to I_{DDQ} Testing, Luwer Academic Publishers, Boston (1977)); and a transient current test is described by, e.g., M. Sachdev., P. Jamssen and V. Zieren ("Defect Detection with Transient Current Testing and its Potential for Deep SubMicron ICs" Proceedings of IEEE International Test Conference (1998):204-213 and Y. Min and Z. Li ("I_{DDT} Testing Versus I_{DDQ} Testing Journal of Electronic Test: Theory and Applications (JETTA) 13(1) (August, 1998):51-56. /4

In order to facilitate testing of a circuit being tested, moreover, a test-facilitating design technique, which affords testing functions to the circuit being tested such as, such as a technique (BIST: built-in self test) to integrate a self-testing function into the circuit being tested, a test point insertion to improve the controllability and the observability of an internal state of the circuit, the scan design technique, the boundary scan, and the like. A test facilitating design technique is given, for example, in chapters 9, 10 and 11 by M. Abramovivi, M.A. Breuer and A.D. Friedman (Digital Systems Testing and Testable Design, IEEE Press, New York, 1990).

However, as the circuit integration level rises to a system LSI, for example, in which a memory, MPU, DSP, I/O interface, and the like are integrated into a single chip, the number of faults subject to tests such as the stuck-at fault test, the delay fault test and the quiescent power supply current test, will be enormous, prohibiting a testing of /5 all of these faults in a practicable length of time. In addition, in the exhaustive test, the state number corresponding to the number of internal flip-flops increases as an exponential function, making it very difficult to carry out such a test. Furthermore, as the circuit scale increases, an increase in the number of functions contained in the circuit being tested results in a tremendous figure for the number of test patterns which are required to test every function in the circuit.

As described above, in order to test the functions of the circuit being tested by the final test, an increased length of time is required,

and the testing cost of the final test increases. On the other hand, a large-scale integrated circuit cannot be subjected to testing all of the stuck-at faults, delay faults and short-circuit faults, presenting a problem that a high fault coverage rate cannot be obtained.

Furthermore, since the rate of increase in the number of pins of an IC package is low in comparison to the rate of improving the integration level of a semiconductor integrated circuit, an external access to signal lines within the circuit will be further difficult in the future, making the final test of the semiconductor integrated circuit very expensive.

In addition, the prior art procedure of testing the semiconductor integrated circuit by the final test has problems because it is impossible to detect defects in manufacturing or a malfunction which occurs during the manufacturing steps, that it is difficult to identify a subsystem which is highly likely to give rise to a fault, and that it is difficult to acquire data on a device level or a subsystem level, which are useable in a simulation or a modeling which is intended for purpose of improving a system performance.

On the other hand, although external access is unnecessary in the test-facilitating design technique in which a testing circuit is integrated within the circuit and simplifies an external access or facilitates the testing of the circuit being tested, this technique has problems because of increased overhead for the chip area, degradation in the performance of the semiconductor integrated circuit being tested which is caused by a testing circuit, a fault coverage which is less than desired, an increased

length of time required for the test, and so forth.

Thus, there is a demand for a testing method by which the testing cost can be reduced and a testing method which is capable of improving the fault coverage for a large-scale semiconductor integrated circuit.

It is an object of this invention to provide a method for manufacturing a semiconductor integrated circuit able to reduce the testing cost or able to improve the fault coverage for a circuit being tested.

Disclosure of the Invention

According to the method of the invention, a method for /6 manufacturing a semiconductor integrated circuit with a multilayer wiring structure by repeating a step of stacking wiring layers (an wiring stacking step) a plurality of times after the basic elements have been formed is characterized by comprising a testing step of successively testing one or more sub-circuits which have been interconnected up to at least one or more intermediate wiring stacking steps among the plurality of the wiring stacking steps.

According to this method, the cost of testing a circuit can be reduced, the fault coverage within the circuit can be improved, and a fault-free semiconductor integrated circuit can be manufactured.

It is desirable, moreover, that the above-mentioned testing step in the manufacturing method of this invention be carried out such that during a 1st testing step, one or more sub-circuits which have been interconnected up to the preceding stacking step be tested, and during a succeeding testing step, the interconnection between the sub-circuits

be tested.

It is also desirable that the above-mentioned testing step in the manufacturing method of this invention be carried out such that during a relatively early testing step of a prescribed stack stage, one or more sub-circuits of a relatively small scale which have been interconnected by preceding stacking steps be tested, and during a succeeding testing step for the final layer, a final functional test of an integrated circuit which is finally interconnected be carried out.

It is desirable, moreover, that the manufacturing method of this invention includes a CMP (chemical mechanical polishing) planarizing step to planarize a stacking surface before transferring into a succeeding stacking step subsequent to the testing step.

It is further desirable that the manufacturing method of this invention includes testing of the semiconductor integrated circuit by using the test facilitating design technique in the testing step, and subsequent removal of a wiring to a testing circuit of the test facilitating design technique which is used in the testing step.

It is additionally desirable that the manufacturing method of this invention comprises a step of confirming whether or not a prescribed step has been completed upon termination of a wiring stacking step, transferring to the testing step if the completion has been confirmed, and transferring to a next stacking step if the completion has not been completed; and a step of confirming whether or not the steps of manufacturing a semiconductor integrate circuit have been completed upon termination of

the testing step and transferring to a next stacking step when the steps are not completed.

It is also desirable that the manufacturing method of this invention comprises a step of confirming whether or not a prescribed step has been completed upon termination of a stacking step, transferring to a 1st testing step which tests a plurality of basic elements or sub-circuits which have been formed and interconnected up to the prescribed step when the completion is found, and transferring to a next stacking step when the step has not been completed; a step of transferring to a next stacking step subsequent to the 1st testing step; a step of confirming whether or not a /7
prescribed wiring stacking step has been completed after the 1st testing step, transferring to a 2nd testing step which tests an interconnection for a plurality of wirings between the plurality of sub-circuits which have been connected up to the prescribed stacking step when the step has not been completed, and transferring to a stacking step which follows the 1st testing step when the completion is not found; and a step of confirming whether or not steps of manufacturing a semiconductor integrated circuit have been completed, and transferring to a stacking step which follows the 1st testing step when the steps have not been completed.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a drawing showing functional blocks of a semiconductor integrated circuit having a plurality of sub-circuits; Figure 2 is a cross section showing a multi-layer wiring structure of the semiconductor integrated circuit having the plurality of sub-circuits; Figure 3 is a

drawing showing a plurality of basic logical gates formed by a 1st wiring layer and signal lines appearing on the stacking surface of the 1st wiring layer; Figure 4 is a drawing showing a plurality of sub-circuits formed a 2nd wiring layer and signal lines appearing on the stacking surface of the 2nd wiring layer; Figure 5 is a drawing showing a semiconductor integrated circuit formed from an Nth wiring layer and signal lines appearing on the stacking surface of the Nth wiring layer; Figure 6 shows cross sections illustrating an example of process steps of an interconnecting step; Figure 7 shows cross sections illustrating another example of process steps of an interconnecting step; Figure 8 is a drawing showing the surface of a semiconductor integrated circuit for describing a conventional semiconductor integrated circuit testing method; Figure 9 shows cross sections illustrating a method for testing respective wiring layers which represents an essential part of the method for manufacturing a semiconductor integrated circuit of this invention; Figure 10 is a drawing showing a semiconductor integrated circuit manufactured by the method for manufacturing a semiconductor integrated circuit of this invention; Figure 11 is a drawing showing an example of a 16-bit counter manufactured in the method for manufacturing a semiconductor integrated circuit of this invention; Figure 12 is a drawing showing a state during the manufacture of the 16-bit counter where 4-bit counters, which are sub-circuits, are formed; Figure 13 is a drawing showing an example of VCO circuit /8 having a DFT circuit; Figure 14 is a drawing showing a VCO circuit which is reconfigured by the method for manufacturing a semiconductor integrated

circuit of this invention; Figure 15 is a drawing showing an example of a digital integrated circuit having a DFT circuit; Figure 16 is a drawing showing a digital integrated circuit which corresponds to Figure 15 reconfigured according to the method for manufacturing a semiconductor integrated circuit of this invention; Figure 17 is a flowchart showing a processing procedure of the method for manufacturing a semiconductor integrated circuit of this invention; Figure 18 is a flowchart showing another processing procedure in the method for manufacturing a semiconductor integrated circuit of this invention; Figure 19 is a flowchart showing a yet another processing procedure in the method for manufacturing a semiconductor integrated circuit of this invention; Figure 20 is a flowchart showing still another processing procedure in the method for manufacturing a semiconductor integrated circuit of this invention; Figure 21 is a flowchart showing even yet another processing procedure in the method for manufacturing a semiconductor integrated circuit of this invention; and Figure 22 is a flowchart showing even still another processing procedure in the method for manufacturing a semiconductor integrated circuit of this invention.

Preferred Embodiment for Carrying out the Invention

According to the method for manufacturing a semiconductor integrated circuit of this invention, after a prescribed intermediate stacking step or in the course of such step, a test is carried out by placing a probe in contact with signal line(s) appearing on the stacking surface by using a probing means, such as a probe card. For example, a test for the level of basic logical gates on the stacking surface of a 1st wiring layer as

shown in Figure 9(a), a test for the level of relatively small scale sub-circuits on the stacking surface of a 2nd wiring layer as shown in Figure 9(b), or a test for the level of larger scale sub-circuits on the stacking surface of an i^{th} wiring layer as shown in Figure 9(c) may take place, and as required, a test of an overall semiconductor integrated circuit is performed on the stacking surface of an N^{th} wiring layer. Furthermore, before the 1st wiring layer is stacked, a test for the level of basic elements or a measurement of element parameters of basic elements may occur by placing a probe in contact with a substrate. A suitable value may be chosen for the number **N** of the interconnected layers, depending on the scale and the layered structure of the circuit.

According to such a method for manufacturing a semiconductor integrated circuit of this invention, the cost for testing a semiconductor integrated circuit can be reduced. The testing cost will be represented here in terms of the number of test patterns.

An exhaustive test for a semiconductor integrated circuit **B** shown in Figure 10 may be considered. The exhaustive test is a method which tests output responses of a circuit being tested for every combination of signal values at input terminals of the circuit being tested and at flip-flops. The semiconductor integrated circuit B comprises combinatorial circuits **C1**, **C2**, **C3** and **C4** which do not contain flip-flops and **m** number of flip-flops circuits **F1**, **F2**, . . . , **Fm**, all of which represent sub-circuits. Assuming the semiconductor integrated circuit B has a number of input terminals is defined as **t**, and numbers of input signal lines

of the combinatorial circuits or sub-circuits **C1**, **C2**, **C3**, **C4** are defined as **p**, **q**, **r** and **s**, respectively (in the example shown in Figure 10, t=7, m=8, p=4, q=3, r=5, s=3). When the circuit is divided into combinatorial circuits and the flip-flops in the manner mentioned above, there is the following relationship between **t**, **m**, **p**, **q**, **r** and **s**:

$$t+m \geq p+q+r+s \quad (1)$$

In the exhaustive test of the semiconductor integrated circuit **B**, it is necessary to test all the combinations of logical signal values in **t** number of input terminals and **m** number of flip-flops; hence, the number of tests amounts to 2^{t+m}. Consequently, if a single test can be tested with a single test pattern, the number of test patterns N(B) will be 2^{t+m}.

$$N(B)=2^{t+m} \quad (2)$$

On the other hand, according to the method for manufacturing a semiconductor integrated circuit of this invention, when a sub-circuit is tested each time such a sub-circuit is formed, and similarly, when each flip-flop is tested each time it is formed to perform the exhaustive test for the respective sub-circuits, the numbers of test patterns **N(C1)**, **N(C2)**, **N(C3)**, **N(C4)**, **N(F1)**, **N(F2)**, ..., **N(Fm)** are:

$$N(C1)=2^{p} \quad (3)$$
$$N(C2)=2^{q} \quad (4)$$
$$N(C3)=2^{r} \quad (5)$$
$$N(C4)=2^{s} \quad (6)$$
$$N(F1)=2^{2+1} \quad (7)$$
$$N(F2)=2^{2+1} \quad (8)$$
$$N(Fm)=2^{2+1} \quad (9).$$

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In addition, because the flip-flop has two inputs and two internal states, the number of test patterns therefor will be equal to 2^{2+1}. As a consequence, the number of test patterns **N** (Bsub) required to perform the exhaustive test for the level of sub-circuits is:

$$N(Bsub)=2^p+2^q+2^r+2^s+8m \qquad (10)$$

Therefore, the number of test patterns in the testing step used in the method for manufacturing a semiconductor integrated circuit of this invention can be reduced from the number of test patterns in the conventional test for the semiconductor integrated circuit by:

$$N(B)-N(Bsub)=2^{t+m}-(2^p+2^q+2^r+2^s+8m).$$

(According to the equation (1), when **t** and **m** are sufficiently large, N(B)-N(Bsub) will be positive.) For example, in the example where t=7, m=8, p=4, q=3, r=5 and s=3, the number of test patterns **N** (Bsub) for the exhaustive test with respect to the 2^{nd} wiring layer is as small as 120, as contrasted to the number of test patterns N(B)=32768 for the uppermost layer, the number of test patterns can be reduced as much as 32648 (approximately 99.6% of N(B)).

According to the method for manufacturing a semiconductor integrated circuit of this invention, after a test for the level of sub-circuits is carried out, the sub-circuits should be tested as to whether they are properly interconnected in the testing step for each wiring layer up to the uppermost layer. Since the interconnection of the wiring being tested should be tested by observing the propagated logical signal value, the number of test patterns which are required therefor is sufficiently small,

as compared with the number of test patterns used in the test of sub-circuits.

In another example, the functional test of a 16-bit counter comprising a semiconductor integrated circuit shown in Figure 11 may be considered. The 16-bit counter has four 4-bit counters **S1**, **S2**, **S3** and **S4** as sub-circuits. /11

In the functional test of the 16-bit counter, it is necessary to see if the 16-bit output properly counts from 0000000000000000 to 1111111111111111; hence, the test requires a number of clocks (test patterns) which is 2^{16}=65536.

On the other hand, according to the method for manufacturing a semiconductor integrated circuit of this invention, when a k^{th} wiring layer is formed to constitute 4-bit counters (sub-circuits) **S1**, **S2**, **S3** and **S4**, as shown in Figure 12, a probe is placed in contact with an input and output signal line of each 4-bit counter which appear on the stacking surface of the k^{th} wiring layer to perform a functional test of each of four sub-circuits **S1**, **S2**, **S3** and **S4**. At this time, it is only required to see if a 4-bit output from each 4bit counter properly counts from 0000 to 1111, and accordingly, the test each requires 2^4=16 clocks (test patterns).

Consequently, the number of test patterns used in the testing step in the method for manufacturing a semiconductor integrated circuit of this invention can be reduced from the number of test patterns which are necessary when performing a test of 16-bit counter by an amount which is equal to 65536-4×16=65472 (99.9%).

The effect of reducing the testing cost will be more remarkably manifested for a large-scale circuit. In addition, such an effect is not limited to the exhaustive test or functional test. A similar effect can also be obtained for the stuck-at fault test, the delay fault test, the quiescent power supply current test, the transient power supply current test, etc.

In addition, in the method for manufacturing a semiconductor integrated circuit of this invention, because each sub-circuit is tested separately during the testing step, when a plurality of sub-circuits are constructed, these plural sub-circuits may be tested in parallel, thus allowing the testing time to be further reduced. Since the sub-circuits operate independently from each other unless they are interconnected, as shown in Figure 4, a parallel test can be made by placing probes simultaneously in contact with a plurality of sub-circuits which appear on the same stacking surface.

In addition, according to the method for manufacturing a semiconductor integrated circuit of this invention, because a testing step is interposed in the course of the multi-layer stacking steps, the fault coverage can be improved and the reliability of the semiconductor integrated circuit can be improved. As the integration level of the circuit is increased, the number of stuck-at faults, which are subject to the stuck-at /12 fault test, increases, and this combined with the presence of flip-flops in a sequential circuit makes access to faulty locations within the circuit difficult. That is, because this requires a test pattern, which is used

to set respective flip-flops with prescribed signal values and other test patterns which propagate the influence of stuck-at fault to an output terminal through a plurality of flip-flops, the number of test patterns required to carry out the stuck-at fault test will be enormous, making it difficult to apply the stuck-at fault test to a large scale integrated circuit so that the test can be completed within a practicable length of time. Thus, a functional test is applied in place of the stuck-at fault test in order to test a large scale integrated circuit, but because the functional test is not explicitly designed to test the stuck-at faults, it is impossible to achieve a satisfactory fault coverage for stuck-at faults.

However, according to the method for manufacturing a semiconductor integrated circuit of this invention, by interposing a testing circuit in units of sub-circuits when smaller scale sub-circuits are constructed during the course of the manufacturing steps, a stuck-at fault test may be to be carried out for each sub-circuit within a practical length of time and the fault coverage for the stuck-at faults for the entire circuit may be improved.

In a CMOS integrated circuit, as the miniaturization of circuit elements (MOS transistors) and higher integrated of the circuit proceed, leakage current from a transistor increases; hence, the quiescent power supply current for the entire chip increases, and an increase in the quiescent power supply current which is caused by a single fault cannot be detected. Thus, the quiescent power supply current test is very difficult in the

larger scale CMOS integrated circuit. However, according to the method for manufacturing a semiconductor integrated circuit of this invention, a test in units of sub-circuits may be performed when smaller scale sub-circuits are formed; hence, the quiescent power supply current test can be carried out for each sub-circuit and the rate for detecting short-circuit faults and/or leakage faults with respect to the entire circuit can be improved. Such an effect is not limited to the stuck-at fault test or the quiescent power supply current test; a similar effect also can be obtained with respect to the delay fault test, the functional test, the exhaustive test, the transient power supply current test, and the like.

Moreover, according to the method for manufacturing a semiconductor integrated circuit of this invention, by performing a test during the steps of manufacturing a circuit, an early detection of defects in manufacturing, such as disconnection faults or short-circuit faults, and/or malfunctioning which results in an out-of-specification circuit performance, and a succeeding testing step or manufacturing steps may be eliminated therefor; hence, the testing cost and the manufacturing cost for the semiconductor integrated circuit may be reduced. /13

In addition, according to the method for manufacturing a semiconductor integrated circuit of this invention, a test can be performed in units of sub-circuits when the sub-circuits are constructed or in units of sub-systems when these sub-systems (relatively large-scale sub-circuits) are constructed so a sub-system or sub-systems can be identified, which

are highly likely to give rise to a failure, and such information can be utilized to add the test facilitating design technique, the scan design technique or the integrated self test (BIST) technique or to improve the reliability of the entire system; hence, a lengthy system repair interval (a time interval needed for repairing a faulty system into a normal system) can be reduced. The test facilitating design techniques are described by, e.g., M. Abramovici, M.A. Breuer and A.D. Friedman (in chapters 9, 10, 11 of Digital Systems Testing and Testable Design, IEEE Press, New York, 1990).

Moreover, it is necessary to collect performance data, such as delay times or current driving capabilities on a device level or on a sub-system level, in a simulation or a modeling to improve system performance. According to the method for manufacturing a semiconductor integrated circuit of this invention, since a test can be carried out in units of devices or units of sub-circuits the steps of manufacturing the circuit, performance data at the device level or the sub-system level can be acquired.

In addition, according to the method for manufacturing a semiconductor integrated circuit of this invention, an appropriate test can be applied in units of sub-circuits; hence, it is not necessary to insert a testing circuit according to the test facilitating design techniques into the integrated circuit, and an area overhead owing to such testing circuit may be reduced.

Furthermore, according tot the method for manufacturing a semiconductor integrated circuit of this invention allows, by effectively utilizing

a CMP (chemical mechanical polishing) planarizing step, a degradation in the performance of the semiconductor integrated circuit caused by the insertion of the testing circuit may be prevented even if the test facilitating design technique is combined.

For example, a test facilitating design technique as shown in Figure 13 has been proposed in order to facilitate a testing of a phase-locked loop (PLL). This method is described by, e.g., F. Azais, M. Renovell, Y. Bertrand, A. Ivanov and S. Tabatabaei ("A Unified Digital Test /14 Technique for PLLs: Catastrophic Fault Covered" Proceedings of 5th IEEE International Mixed Signal Testing Workshop (June 1999): 269-292. This method is one in which two MOSFETs (M1, M2) are inserted as the test-facilitating circuit (DFT: Design for Test) between an input stage and an input of a voltage-controlled oscillator (VCO) which forms the PLL circuit. During a normal operation, the MOSFET **M1** is turned ON while the MOSTET **M2** is turned OFF, and an input into an output buffer is inputted into the input stage of the oscillator circuit, or a feedback loop **FL** is closed to form the VCO circuit. During the test, the **M1** is turned OFF while the **M2** is turned ON to disconnect the feedback loop **FL** in the VCO circuit, thus activating a path from the input terminal **IN** to an output terminal **OUT** for carrying out a test. However, since the MOSFET (M1) is inserted into the feedback loop **FL** of the VCO circuit according to this procedure, a problem is presented because the resistance of the MOSFET lowers the operational speed of the PLL circuit during the normal operation.

Vis-à-vis, according to the method for manufacturing a semiconductor integrated circuit of this invention, after a wiring layer which connects the **M1** and **M2** as shown in Figure 13 has been formed, a test was performed on the PLL circuit being tested by placing a probe in contact with the wiring in the PLL being tested to turn the **M1** OFF and to turn the **M2** ON, and after the PLL circuit being tested has been tested, the wiring to the testing circuits **M1** and **M2** shown in dotted lines may be removed by CMP and a new wiring **L1** shown by solid line may be stacked, as shown in Figure 14, to be able to reconfigure a feedback loop in which the **M1** is removed and manufacturing a PLL circuit free from a degradation in the performance. In other words, a wiring layer which comprises wirings shown by the dotted lines in Figure 14 is formed to provide a circuit arrangement shown in Figure 13 to perform a test, and upon completion of the test, the interconnected layers shown by dotted lines is removed, and a wiring layer which forms the wiring **L1** to constitute the feedback loop is formed thereon. The reconfigured PLL circuit is already tested, and there is an assurance that it operates normally.

A test facilitating design technique, as shown in Figure 15, is moreover proposed to facilitate the delay fault test and the stuck-at fault test of a digital integrated circuit. This procedure is described by, e.g., K. Arabi, H. Ihs, C. Dufaza and B. Kaminska ("Digital Oscillation-Test Method for Delay and Stuck-at Fault testing of Digital Circuits" Proceedings of IEEE International Test Conference (Oct. 1999): 91-100. In this /15 procedure, an input signal line **L2** and an output signal line **L4** of a signal

propagation path being tested of a digital integrated circuit (or more generally, a critical path having a long delay time is selected) are connected through an XOR gate and a multiplexer in loop form as depicted by the thick lines, and during a normal operation, an input **TEST** of the multiplexer is controlled so that the feedback loop is deactivated to connect **B1** to **L2** and operate the circuit being tested, and during the test, a multiplexer **MUX** is controlled to connect the output of the XOR gate to the input line **L2** and define the loop, and the input **INV** of the XOR gate is controlled to form a ring oscillator including an odd number of output inverting logical gates (output inverting gates) within the loop and test the delay fault and the stuck-at fault on the critical path. Here, the XOR gate is used to control the number of output inverting gates on the feedback loop by providing "1" for the input **INV** to operate it as an output inverting gate when there is even number of output inverting gates on the critical path, and providing "0" for the input **INV** when there are an odd number of output inverting gates on the critical path. For example, in Figure 15, the number of output inverting gates on the critical path is equal to 0, hence, during the test, INV="1" may be inputted. However, because the multiplexer and the XOR gate are connected to the input and the output of the digital semiconductor integrated circuit, there is a problem because the propagation delay time of the multiplexer **MUX** and the parasitic capacitance of the XOR gate lower the operational speed of the digital semiconductor integrated circuit during normal operation.

Vis-à-vis, in the method for manufacturing a semiconductor integrated circuit of the invention, a testing step is executed when a wiring layer which connects the above-mentioned testing circuit **MUX, XOR** is formed. A probe is placed in contact with the wiring in the digital semiconductor integrated circuit, the required input is applied to test the digital semiconductor integrated circuit, and subsequently, the testing circuit shown by the dotted lines in Figure 16, namely, the wiring layer leading to the **MUX** and **XOR** is removed by CMP, and a new input signal line shown by a thick solid line is stacked. By the above process, a digital semiconductor integrated circuit which has been tested without accompanying degradation in performance caused by the **MUX** and **XOR** can be manufactured. Here, the digital semiconductor integrated circuit which is reconfigured in this manner is already tested, and is assured to operate in a normal manner. /16

It is desirable that a semiconductor integrated circuit having a multilayered wiring structure which is subject to the manufacture of this invention be a damascene wiring structure. A damascene wiring structure is described by, e.g., A.K. Stamper, T.L. McDevitt, and S.L. Luce ("Sub-0.25-micron Interconnection Scaling: Damascene Copper versus Subtractive Aluminum" IEEE/SEMI Advanced Semiconductor Manufacturing Conference, (1998): 337-346. The wiring material is not limited to the copper (Cu), but may be copper-magnesium (Cu-Mg). With a semiconductor integrated circuit having a damascene wiring structure, subsequent to a prescribed stacking step and before transferring to a succeeding stacking

step, step of planarizing the stacking surface as shown in Figure 6(g), for example, a CMP planarizing step is performed. According to the planarizing step, a miniscule scar of contact, such as a minute dimple, which may be formed when a probe is placed in contact therewith during the testing step at an intermediate stage, which constitutes an essential feature of this invention, can be removed; hence, the testing step from out of the manufacturing steps can be executed without affecting the steps for manufacturing a semiconductor integrated circuit.

Moreover, a semiconductor integrated circuit having a multilayer wiring structure which is subject to the manufacture of this invention is not limited to a digital circuit; it may be an analog circuit or a mixed signal circuit comprising a mixture of a digital circuit and an analog circuit.

In addition, a semiconductor integrated circuit having a multilayer wiring structure which is subject to manufacture according to the present invention is not limited to single substrate semiconductor integrated circuit; it may be a semiconductor integrated circuit which is executed three- dimensionally by stacking a plurality of sub-substrates.

Furthermore, the semiconductor integrated circuit having a multilayer wiring structure which is subject to the manufacture according to the present invention is not limited to a single chip semiconductor integrated circuit; it may be a semiconductor integrated circuit obtained by integrating a plurality of sub-chips by using a common multi-layer wiring structure.

The practical examples of a processing procedure of the method of this invention will now be described.

Figure 17 shows an example of a processing procedure of the method for manufacturing a semiconductor integrated circuit of this invention. Firstly, in step 101, a step of forming basic elements (transistors, etc.) in a semiconductor substrate is performed. In step 102 next, whether or not signal lines are formed on a layer surface is confirmed, and /17 if they are not formed, a wiring stacking step shown in step 103 is used to form signal lines, and if the signal lines are formed, the operation proceeds to step 104.

In step 104, whether or not at least one prescribed step which is predetermined during the manufacture is completed is confirmed, and if the prescribed step is not completed, the wiring stacking step in step 103 is repeated, and if the prescribed step has been completed, the operation proceeds to step 105. The wiring stacking step in step 103 comprises a step of stacking a wiring layer for basic elements and sub-circuits and may comprise process steps shown in Figure 6, for example. Subsequently, in step 105, a plurality of basic elements or sub-circuits which have been formed and interconnected up to said step are tested sequentially or in parallel. Finally, in step 106, whether or not the steps of manufacturing a semiconductor integrated circuit have been completed is confirmed. If the manufacturing steps have not been completed, the steps 102, 103, 104 and 105 are repeated, and if the manufacturing steps have been completed, the processing ends. The above-mentioned testing step

in step 105 may include a test for basic elements, a test for small sub-circuits, a test for relatively large sub-circuits, or the like, depending on the interconnection which has been completed thus far, and is carried out each time each wiring layer, such as the 2nd and a subsequent wiring layer is formed. The testing of basic elements or sub-circuits may use an exhaustive test, a functional test, a stuck-at fault test, a delay fault test, a quiescent power supply power current test, a transient power supply current test, a parametric test or any other testing method. In particular, a test performed after the formation of each wiring layer subsequent to the initial test may just be a wiring connection test.

Figure 18 shows another example of a processing procedure of the method for manufacturing a semiconductor integrated circuit of this invention. Firstly, in step 201, a step of forming basic elements (such as transistors) in a semiconductor substrate is performed. Then in step 202, whether or not signal lines are formed on the surface of the wiring layer is confirmed, and if the signal lines are not formed, the signal lines are formed in the wiring stacking step (1st half) in step 203 by the process shown in Figures 7(a) to (c), for example, and if the signal lines are formed, the operation proceeds to step 204. Then in step 204, whether or not a prescribed step (not limited to one) has been completed is confirmed, and if the prescribed step has not been completed, the /18 operation proceeds to the interconnect stacking step (2nd half) in step 206. However, if the prescribed step in step 204 has been completed, a plurality of basic elements or sub-circuits which have interconnected

are tested sequentially or in parallel in step 205. Subsequently, in step 206, a wiring stacking step (2nd half), such as the process shown in Figures 7(d) and (e), is performed to complete the interconnecting step. Finally in step 207, whether or not the steps of manufacturing a semiconductor integrated circuit have been completed is confirmed, and if the manufacturing steps have not been completed, the steps 202, 203, 204, 205 and 206 are repeated, and if the manufacturing steps have been completed, the processing ends. In the testing step in step 205, the test of basic elements or sub-circuits may use an exhaustive test, a functional test, a stuck-at fault test, a delay fault test, a quiescent power supply current test, a transient power supply current test, a parametric test, a wiring connection test or any other testing method.

Figure 19 shows yet another example of a processing procedure of the method for manufacturing a semiconductor integrated circuit of this invention. Firstly, in step 301, a step of forming basic elements (such as transistors) in a semiconductor substrate is performed. Then, in step 302, a test for the level of basic elements or a parametric test which measures the element parameters of basic elements is performed. Then, in step 303, signal lines are formed by a wiring stacking step, and in step 304, whether or not the signal lines are formed on the stacking surface is confirmed, and if the signal lines are not formed, the operation returns to step 303, and if the signal lines are formed, the operation proceeds to step 305. In step 305, whether or not a prescribed step (not limited to one) has been completed is confirmed. If the prescribed step has not

been completed, a wiring stacking step in step 303 is repeated, and if the prescribed step has been completed, the operation proceeds to step 306. The wiring stacking step in step 303 is one where the wiring of the basic elements or sub-circuits is performed by stacking, and comprises the process steps as shown in Figure 6, for example. Subsequently, in step 306, a plurality of interconnected basic elements or sub-circuits are tested sequentially or in parallel. Finally, in step 307, whether or not the steps of manufacturing a semiconductor integrated circuit have been completed is confirmed, and if the manufacturing steps have not been completed, the steps 303, 304, 305 and 306 are repeated. If the /19 manufacturing steps have been completed, the processing ends. In the testing step in step 306, a test of basic elements or sub-circuits may use an exhaustive test, a functional test, a stuck-at fault test, a delay fault test, a quiescent power supply current test, a transient power supply current test, a parametric test, a wiring connection test or any other testing method.

Figure 20 shows still another example of a processing procedure of the method for manufacturing a semiconductor integrated circuit of this invention. Firstly, in step 501, a step of forming basic elements (such as transistors) in a semiconductor substrate is performed. Then, in step 502, whether or not signal lines are formed on the stacking surface is confirmed, and if the signal lines are not formed, the signal lines are formed by the wiring stacking step of step 503, and if the signal lines are formed, the operation proceeds to step 504. In step 504, whether

or not a prescribed step has been completed is confirmed, and if the prescribed step has not been completed, the wiring stacking step of step 503 is repeated, and if the prescribed step has been completed, the operation proceeds to step 505. The wiring stacking step of step 503 is one where the wiring for the basic elements or sub-circuits is performed by stacking and which comprises the process steps shown in Figure 6, for example. In step 505 next, a test of the plurality of interconnected basic elements or sub-circuits is performed.

Subsequently, in step 506, a wiring stacking step is performed again. The wiring stacking step of step 506 is a step of forming a wiring layer which wires together the plurality of basic elements or sub-circuits that have been tested up to the step 505 to form a larger scale sub-circuit, and comprises the process steps shown in Figure 6, for example. In step 507 next, whether or not signal lines are formed on the stacking surface is confirmed, and if the signal lines are not formed, the signal lines are formed by the wiring stacking step of step 506. However, if the signal lines are formed, the operation proceeds to step 508. In step 508, whether or not a prescribed stacking step (which is not limited to one) has been completed is confirmed, and if the prescribed stacking step has not been completed, the stacking step of step 506 is repeated, and if the prescribed stacking step has been completed, the operation proceeds to step 509. /20 In step 509, a wiring connection test is performed on a plurality of wirings between a plurality of connected sub-circuits up to the stacking step. Finally, in step 510, whether or not the steps of manufacturing a

semiconductor integrated circuit have been completed is confirmed, and if the manufacturing steps have not been completed, the steps 506, 507, 508 and 509 are repeated, and if the manufacturing steps have been completed, the processing ends. In the sub-circuit testing step of step 505, a test of the basic elements or sub-circuits may use an exhaustive test, a functional test, a stuck-at fault test, a delay fault test, a quiescent power supply current test, a transient power supply current test, a parametric test or any other testing method. Furthermore, the sub-circuit testing step of step 505 above may test the plurality of sub-circuits sequentially, or it may test them in parallel. Similarly, the wiring connection testing step of step 509 may test the plurality of wiring connections sequentially or it may test them in parallel. It is preferable that the wiring connection test of step 509 be performed each time a wiring stacking step which follows the step 505 has been completed. In this instance, step 508 may be omitted.

Figure 21 shows still yet another example of a processing procedure of the method for manufacturing a semiconductor integrated circuit of this invention. Firstly, in step 601, a step of forming basic elements (such as transistors) on the semiconductor substrate during the steps of manufacturing a semiconductor integrated circuit is performed. In step 602 next, whether or not signal lines are formed on the stacking surface is confirmed, and if the signal lines are not formed, the operation proceeds to a wiring stacking step of step 605, and if the signal lines are formed, the operation proceeds to step 603. In step 603, whether or not a prescribed step (which is not limited to one) has been completed

is performed, and if the prescribed step has not been completed, the operation proceeds to the wiring stacking step of step 605, and if the prescribed step has been completed, the operation proceeds to step 604. In step 604, a test of the plurality of the interconnected basic elements or sub-circuits is performed.

Then in step 605, a wiring stacking step is performed for form signal lines on the surface of the wiring layer. It is to be noted that the wiring stacking step of step 605 is one in which a wiring between the basic elements or sub-circuit is performed by stacking, and which comprises the process steps shown in Figure 6, for example. In step 606 next, whether or not the steps of manufacturing a semiconductor integrated circuit /21 have been completed is confirmed, and if the manufacturing steps have not been completed, the steps 602, 603, 604 and 605 are repeated, and if the manufacturing steps have been completed, the operation proceeds to step 607. Finally, in step 607, a final functional test (functional test) of finally integrated semiconductor integrated circuit is performed to end the processing. In the sub-circuit testing step of step 604, a test of the basic elements or sub-circuits may use an exhaustive test, a functional test, a stuck-at fault test, a delay fault test, a quiescent power supply current test, a transient power supply current test, a parametric test or any other testing method. Furthermore, the sub-circuits testing step of step 604 may test the plurality of sub-circuits sequentially or it may test them in parallel. Moreover, the final functional testing step of step 606 may use a testing method other than the functional test,

as needed. The final test of step 607 may be performed by placing a probe in contact with a bonding pad on the semiconductor integrated circuit, or may be performed on a packaged semiconductor integrated circuit.

Figure 22 shows even yet another example of a processing procedure of the method for manufacturing a semiconductor integrated circuit of this invention. Firstly, in step 801, a step of forming basic elements (such as transistors) on a semiconductor substrate is performed. Then, in step 802, whether or not signal lines are formed on the wiring surface is confirmed, and if the signal lines are not formed, the signal lines is formed by a wiring stacking step of step 803, and if the signal lines are formed, the operation proceeds to step 804. In step 804, whether or not a prescribed step (which is not limited to one) has been completed is confirmed, and if the prescribed step has not been completed, the wiring stacking step of step 803 is repeated, and if the prescribed step has been completed, the operation proceeds to step 805.

Here, the wiring stacking step of step 803 is one in which the wiring for the basic elements or sub-circuits is performed by stacking and comprises the process steps shown in Figure 6, for example. In step 805 next, a test of the plurality of basic elements or sub-circuits which have been formed and interconnected is performed. In step 806 next, a CMP planarizing step is performed. The purpose of CMP planarizing step 806 is to remove minuscule scars of contact which may be formed when a probe is placed in contact at the testing step 805 or to remove a wiring to the testing circuit for the test facilitating design technique used in

/22

the testing step 805. Finally, in step 807, whether or not the steps of manufacturing a semiconductor integrated circuit have been completed is confirmed, and if the manufacturing steps have not been completed, the steps 802, 803, 804, 805 and 806 are repeated, and if the manufacturing steps have been completed, the processing ends. In the testing step of step 805, the test of the basic elements or the sub-circuits may use an exhaustive test, a functional test, a stuck-at fault test, a delay fault test, a quiescent power supply current test, a transient power supply current test, a parametric test, a wiring connection test or any other testing method. Furthermore, the testing step of step 805 may test the plurality of sub-circuits sequentially or it may test them in parallel.

The wiring stacking step in steps 503 and 506 in Figure 20, step 605 in Figure 21 and step 803 in Figure 22 may use the process shown in Figure 7. In this case, the wiring stacking step may be divided into a 1st-half step and a 2nd-half step, as shown in the practical example in Figure 18, and a case in which the test is performed at a prescribed step, it may be performed after the completion of the 1st-half step, and may be followed by the 2nd-half step.

As described above, according to the method for manufacturing a semiconductor integrated circuit of this present invention, a semiconductor integrated circuit having a multilayer wiring structure is tested in units of sub-circuits may be performed from out of the steps of manufacturing the circuit; hence the number of test patterns and the testing cost can be reduced to provide a significant improvement in the economical advantages

of a large-scale semiconductor integrated circuit testing

In addition, according to the method for manufacturing a semiconductor integrated circuit of this invention, a test from out of the steps of manufacturing a circuit on a semiconductor integrated circuit having a multilayer wiring structure is done in units of sub-circuits; hence, a testing method inapplicable to a large-scale integrated circuit to be used can be applied, thus significantly improving the fault coverage.

According to the method for manufacturing a semiconductor integrated circuit of this invention as well, by performing a test in units of sub-circuits from out of steps for manufacturing a semiconductor integrated circuit having a multilayer wiring structure thereon, the test-facilitating design technique for improving the ease of testing sub-circuits /23 becomes unnecessary; hence, an area overhead for the testing circuit can be reduced to null.

Moreover, according to the method for manufacturing a semiconductor integrated circuit of this invention, by performing a test in units of sub-circuits from out of the steps of manufacturing a circuit on a semiconductor integrated circuit having a multilayer wiring structure, a parallel testing of wirings between the sub-circuits or between a system and sub-circuits on the same chip as the system functions can be done, and the testing time and testing cost can be reduced and semiconductor integrated circuit free of faults can be manufactured in a short time.

In addition, according to the method for manufacturing a semiconductor integrated circuit of this invention, by doing a test in units of sub-circuits

from out of the steps of manufacturing a circuit on the semiconductor integrated circuit having a multilayer wiring structure; early detection of defects in manufacturing, such as disconnection faults or short-circuit fault, and malfunctioning so as to cause an out-of-specification circuit performance is enabled, and the testing cost and cost for manufacturing the semiconductor integrated circuit may be reduced.

Furthermore, according to the method for manufacturing a semiconductor integrated circuit of this invention, by doing a test in units of sub-circuits from out of the steps of manufacturing a circuit on a semiconductor integrated circuit having a multilayer wiring structure, sub-systems which are highly dangerous in causing failures can be identified, and such information may be used to adding the test facilitating design technique or to improve the reliability of the overall system, a lengthy system repair interval (an interval for repairing a faulty system as a normal system) can be reduced.

Also, according to the method for manufacturing a semiconductor integrated circuit of this invention, by doing a test in units of sub-circuits from out of the steps of manufacturing a circuit on a semiconductor integrated circuit having a multilayer wiring structure, performance data, such as delay times or current driving capabilities on the device level or the subsystem level required in a simulation or modeling to improve the system performance can be acquired.

Moreover, according to the method for manufacturing a semiconductor integrated circuit of this invention, by doing a test in units of sub-circuits

from out of the steps of manufacturing a circuit on a semiconductor integrated circuit with a multilayer wiring structure, acceptable components which satisfy KGD (known good die) standard demands can be ensured after the final test, and the KGD cost can be reduced drastically.

In addition, according to the method for manufacturing a semiconductor integrated circuit of this invention, even if the test facilitating /24
design technique is combined with a semiconductor integrated circuit having a multilayer wiring structure, after the testing circuit according to the test facilitating design technique has been used to perform a test, the wiring for the testing circuit which is used in the testing step may be removed by utilizing a CMP (chemical mechanical polishing) planarizing step to reconfigure the circuit, and degradation in the performance of the semiconductor integrated circuit being tested caused by the test facilitating design technique can be prevented.

Claim(s) /25

1. A method for manufacturing a semiconductor integrated circuit by performing a wiring stacking step a plurality of times after forming basic elements; said method for manufacturing a semiconductor integrated circuit characterized by comprising a testing step of testing one or more basic elements and sub-circuits interconnected in at least one or more wiring stacking steps among the plurality of the wiring stacking steps.

2. The method for manufacturing of a semiconductor integrated circuit of Claim 1; said method for manufacturing a semiconductor integrated circuit characterized by comprising a 1st testing step of performing a test on

at least one interconnected basic element or sub-circuit and a 2nd step of performing an interconnection test on the wiring between the above-mentioned basic element or sub-circuit on the basis of the wiring stacking step after the 1st testing step thereof

3. The method for manufacturing of a semiconductor integrated circuit of Claim 1; said method for manufacturing a semiconductor integrated circuit characterized by comprising a planarizing step to planarize a stacking surface before transferring to a succeeding stacking step subsequent to the above-mentioned testing step.

4. The method for manufacturing of a semiconductor integrated circuit of Claim 1; said method for manufacturing a semiconductor integrated circuit characterized by comprising a step of removing the wiring to the testing circuit according to a test-facilitating design technique used in the above-mentioned testing step after performing testing of the above-mentioned semiconductor integrated circuit using the test-facilitating design technique in the above-mentioned testing step.

5. The method for manufacturing of a semiconductor integrated circuit of Claim 1; said method for manufacturing a semiconductor integrated circuit characterized by comprising a step of confirming whether or not a prescribed step has been completed upon the ending of a wiring stacking step, a step of transferring into a succeeding testing step if the above-mentioned prescribed step has ended, a step of confirming whether or not the step of manufacturing the semiconductor integrated circuit has ended, and if it has ended, transferring into a subsequent stacking step.

6. The method for manufacturing of a semiconductor integrated circuit of Claim 1; said method for manufacturing a semiconductor integrated circuit characterized by comprising a step of confirming whether or not the prescribed step has ended upon ending of the stacking step, transferring into a testing process (1st testing step) on a plurality of basic elements and sub-circuits formed and interconnected thus far if it is confirmed that the above-mentioned prescribed test has ended, and transferring into the subsequent stacking step if the prescribed test has not ended; a step of transferring /26 into a subsequent wiring stacking step if the above-mentioned 1st testing step has ended; a step of confirming whether or not the prescribed stacking step has ended subsequently, and if it is confirmed that the prescribed stacking step has ended, transferring into a 2nd testing step of performing an interconnection test on a plurality of wirings between a plurality of sub-circuits connected thus far, and transferring to the subsequent stacking step if the prescribed stacking steps has not ended; and a step of confirming whether or not the step of manufacturing the semiconductor integrated circuit has ended upon ending of the above-mentioned 2nd testing step, and if it has not ended, transferring into the subsequent stacking step after the above-mentioned 1st testing step.

7. The method for manufacturing of a semiconductor integrated circuit of Claim 1; said method for manufacturing a semiconductor integrated circuit characterized by comprising a step of confirming whether or not a prescribed step has ended in the 1st-half step of the above-mentioned stacking step has ended, and if the prescribed step has not ended, transferring into

a 2nd-half step of the stacking step thereof, and if it is confirmed that the prescribed step has ended, transferring into the above-mentioned testing step; a step of transferring into the 2nd-half of the above-mentioned stacking step if the above-mentioned testing step ends; and a step of confirming whether or not a step of manufacturing a semiconductor integrated circuit has ended if the 2nd-half step of the above-mentioned stacking step ends, and if it has not ended, transferring into the 1st-half step of the subsequent stacking step.

8. The method for manufacturing of a semiconductor integrated circuit of Claim 1; said method for manufacturing a semiconductor integrated circuit characterized by comprising a final testing step of performing a final function test on the stacking circuit finally interconnected in a final stacking step.

9. The method for manufacturing of a semiconductor integrated circuit of Claim 1; said method for manufacturing a semiconductor integrated circuit characterized by comprising a step of performing a parametric test on the above-mentioned basic elements before the above-mentioned wiring stacking step after the above-mentioned formation of the basic elements.

Figure 1

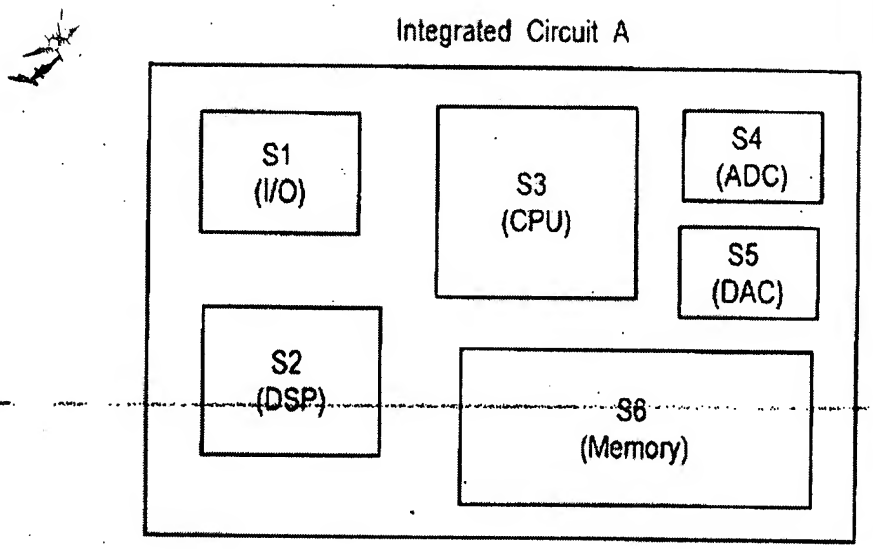


Figure 2

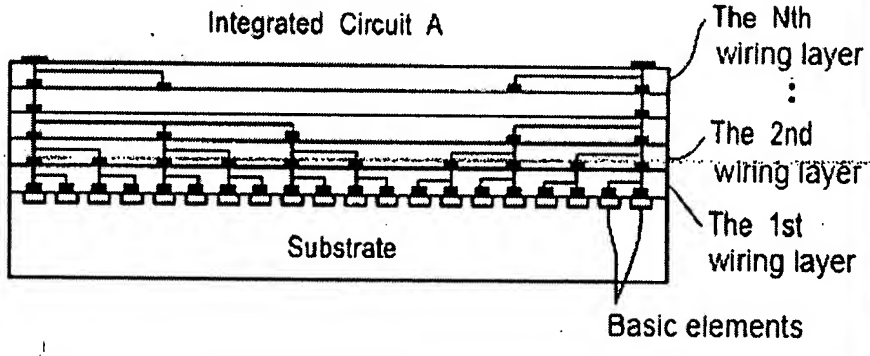


Figure 3

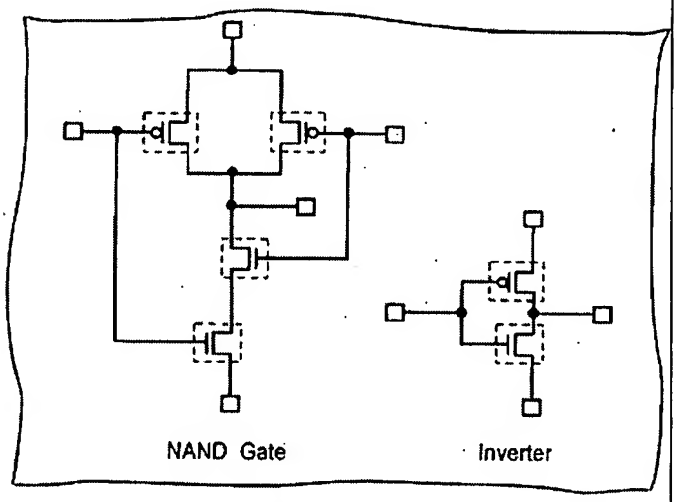


Figure 4

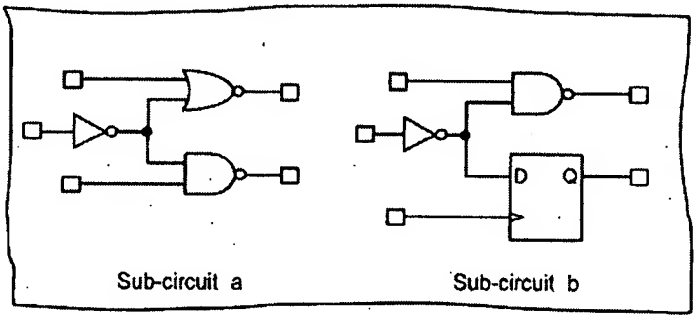


Figure 5

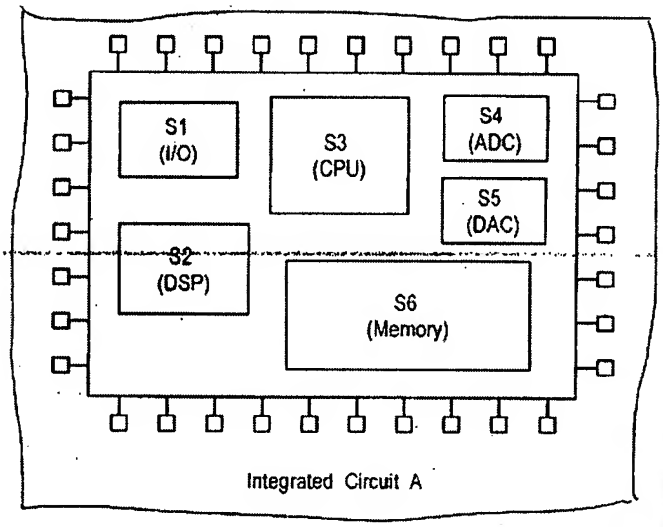
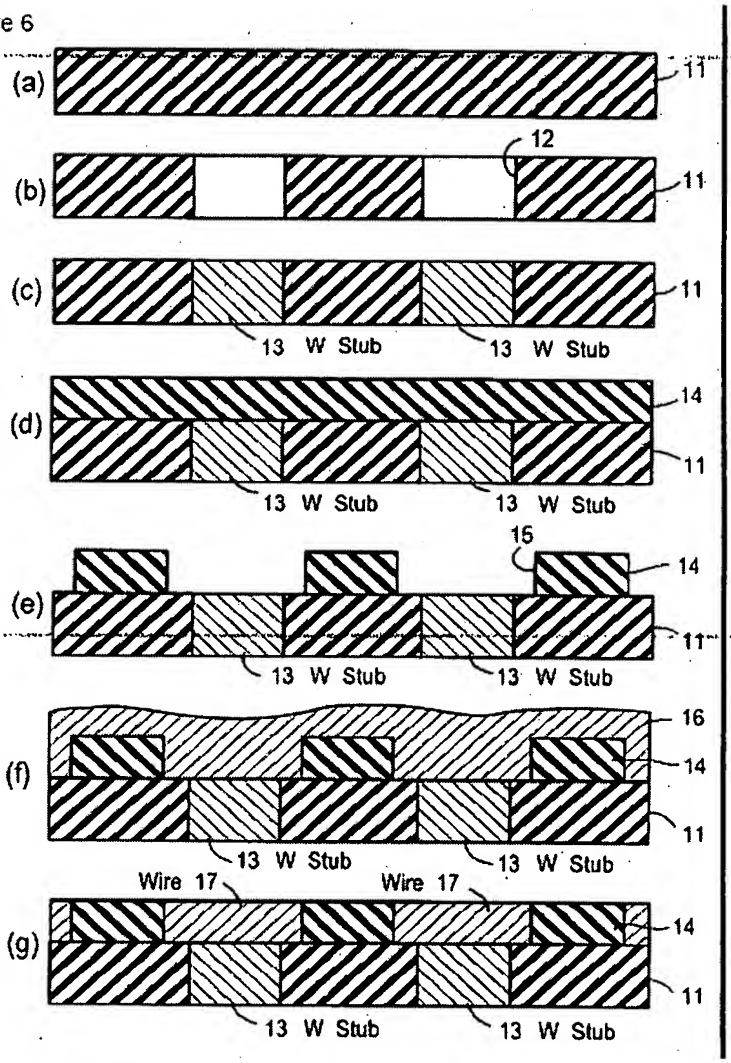

S1
(I/O)
S3
(CPU)
S4
(ADC)
S5
(DAC)
S2
(DSP)
S6
(Memory)
Integrated Circuit A

Figure 6


(a)
11
(b)
12
11
(c)
11
13 W Stub
13 W Stub
(d)
14
11
13 W Stub
13 W Stub
(e)
15
14
11
13 W Stub
13 W Stub
(f)
16
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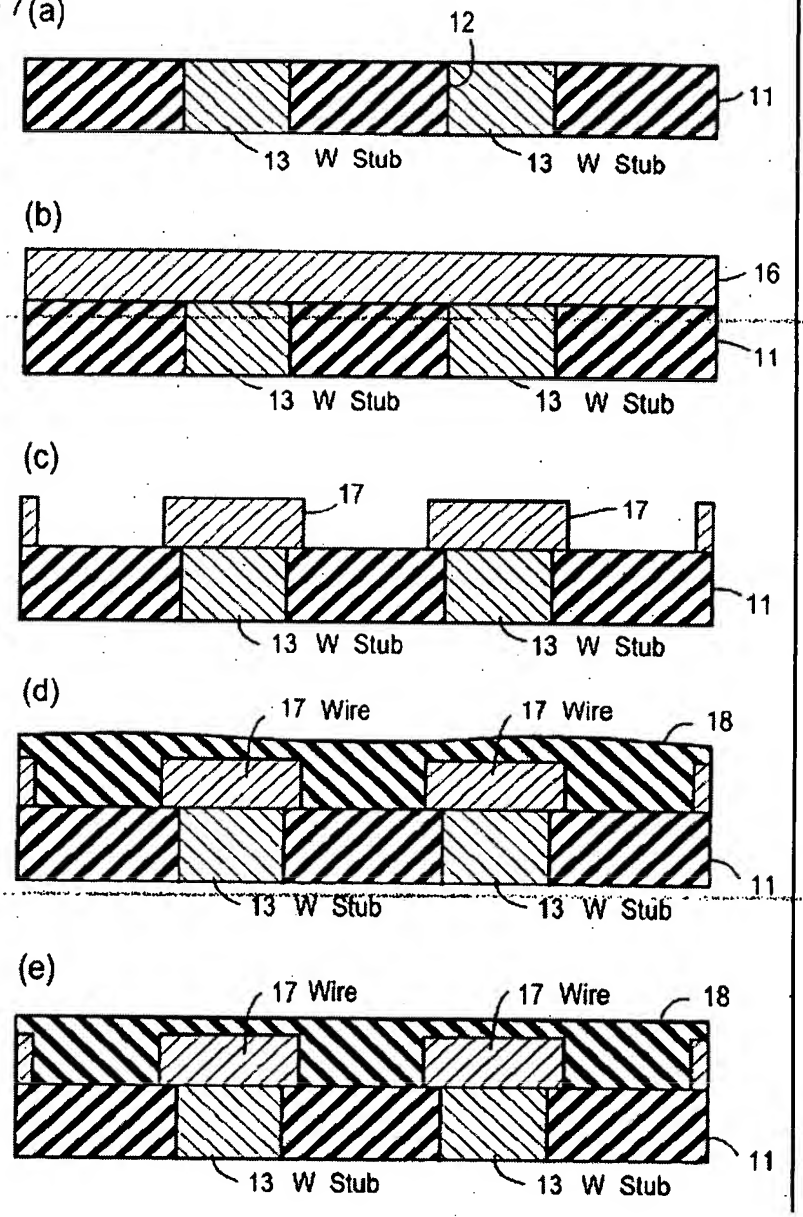
13 W Stub
Wire 17
Wire 17
(g)
14
11
13 W Stub
13 W Stub

Figure 7 (a)


12
11
13 W Stub
13 W Stub
(b)
16
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17
17
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(d)
17 Wire
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(e)
17 Wire
17 Wire
18
11
13 W Stub
13 W Stub

Figure 8

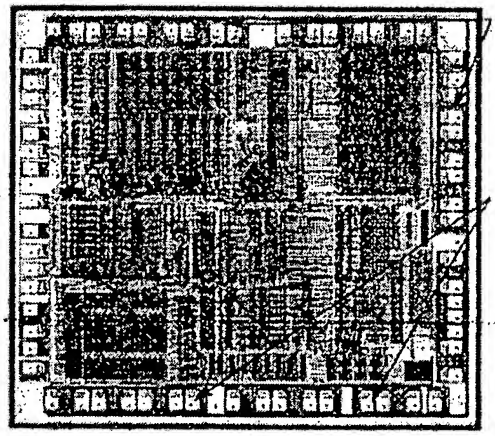

Bond Pads
(I/O pads,
Power supply pads,
and Ground pads)
Probe Marks

Figure 9

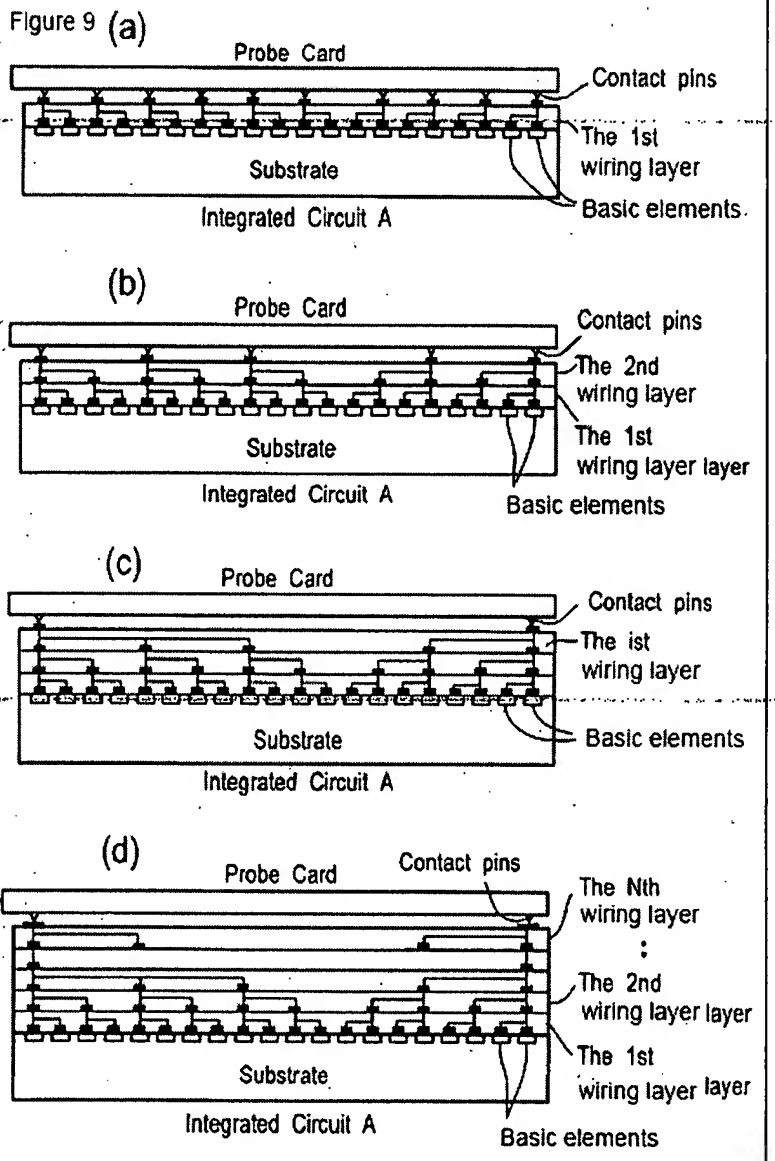
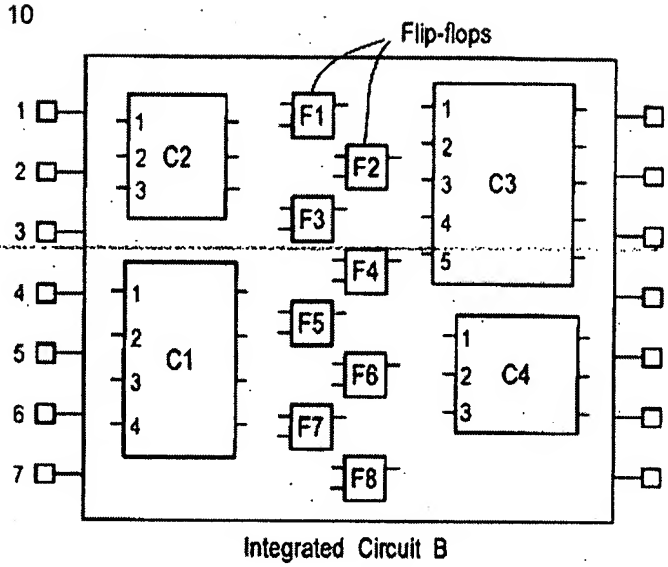
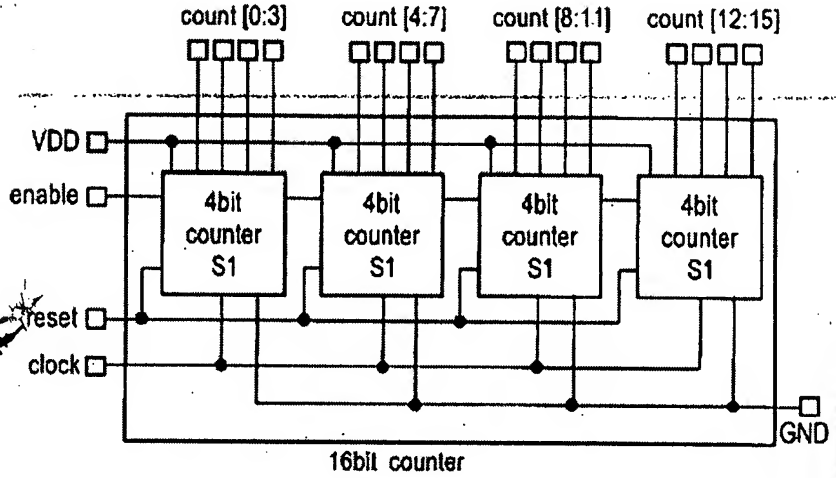

(a)
Probe Card
Contact pins
The 1st
wiring layer
Substrate
Basic elements
Integrated Circuit A
(b)
Probe Card
Contact pins
The 2nd
wiring layer
The 1st
wiring layer layer
Substrate
Integrated Circuit A
Basic elements
(c)
Probe Card
Contact pins
The ist
wiring layer
Substrate
Basic elements
Integrated Circuit A
(d)
Probe Card
Contact pins
The Nth
wiring layer
:
The 2nd
wiring layer layer
The 1st
wiring layer layer
Substrate
Integrated Circuit A
Basic elements

Figure 10



Integrated Circuit B

Figure 11



16bit counter

Figure 12

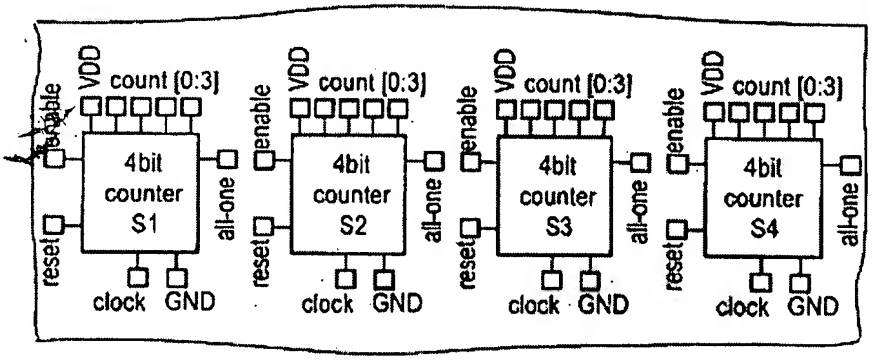


Figure 13

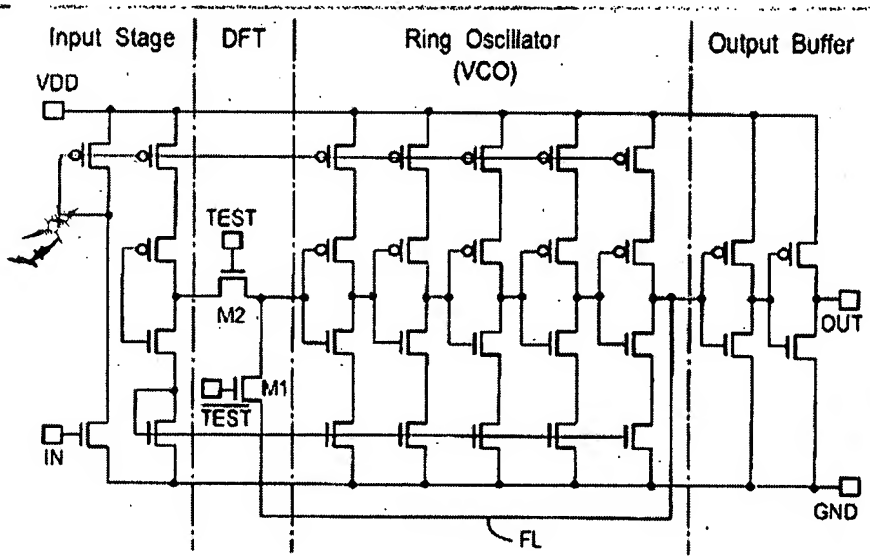


Figure 14

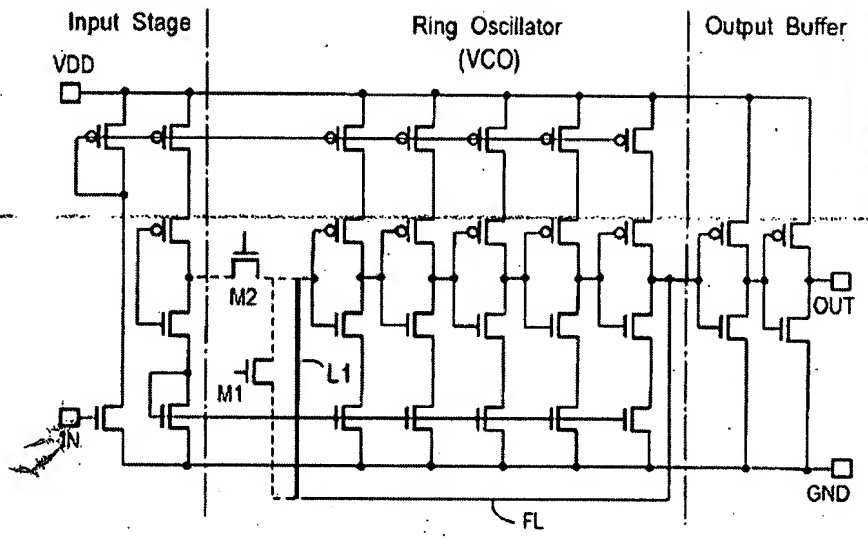


Figure 15

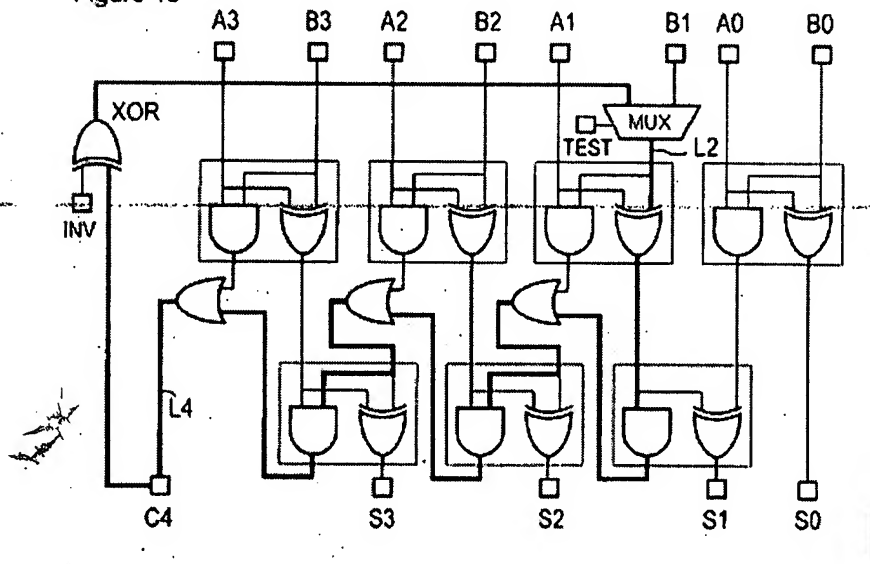


Figure 16

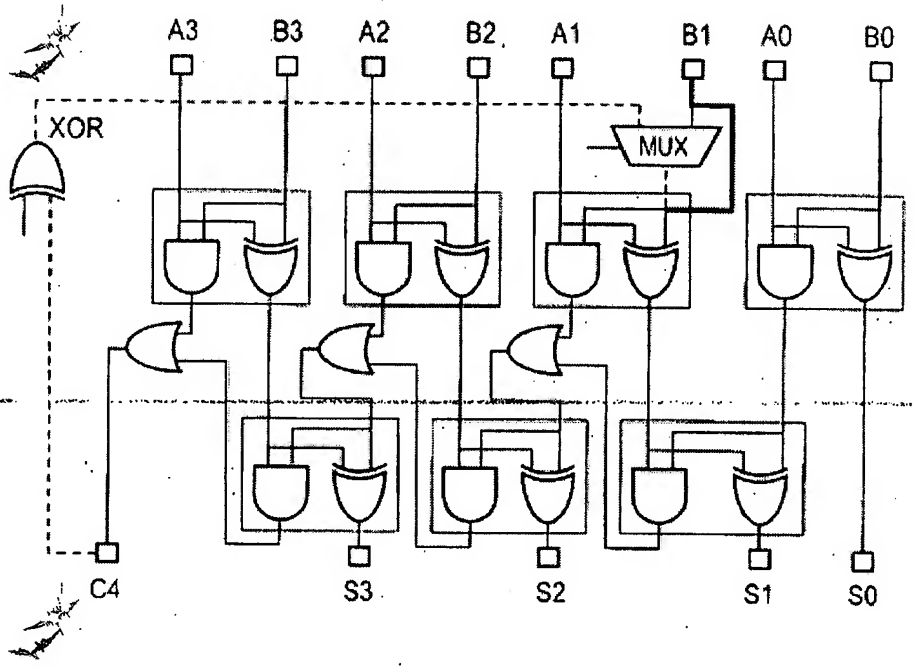


Figure 17

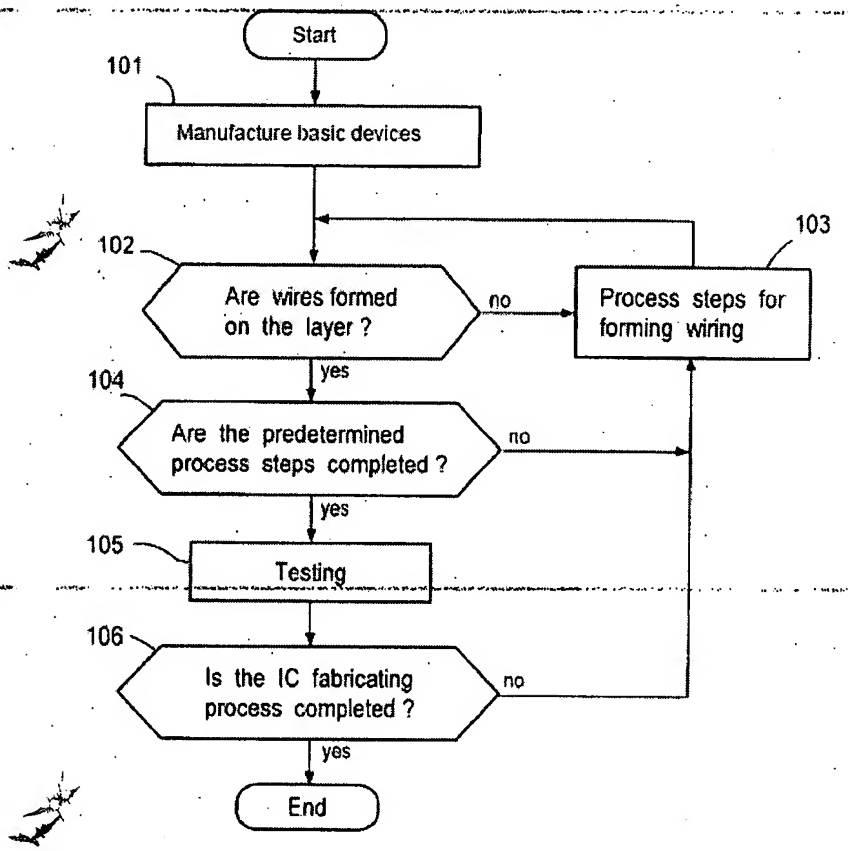

Start
101
Manufacture basic devices
103
102
Are wires formed on the layer ?
no
Process steps for forming wiring
yes
104
Are the predetermined process steps completed ?
no
yes
105
Testing
106
Is the IC fabricating process completed ?
no
yes
End

Figure 18

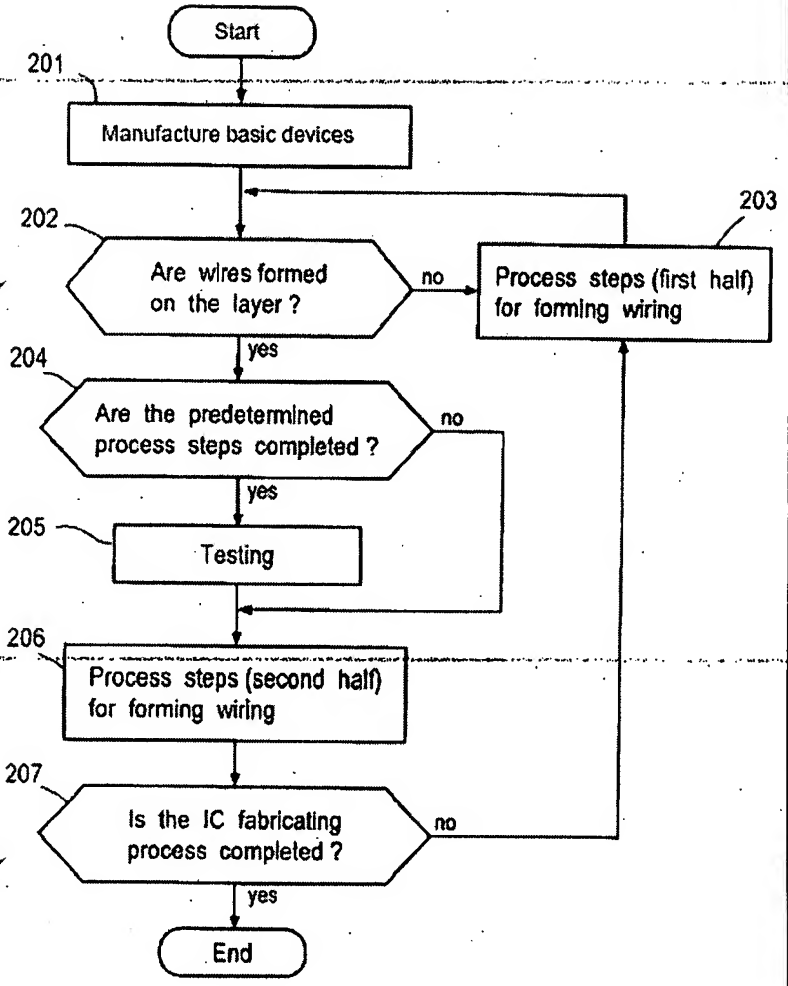

Start
201
Manufacture basic devices
202
Are wires formed on the layer ?
no
203
Process steps (first half) for forming wiring
yes
204
Are the predetermined process steps completed ?
no
yes
205
Testing
206
Process steps (second half) for forming wiring
207
Is the IC fabricating process completed ?
no
yes
End

Figure 19

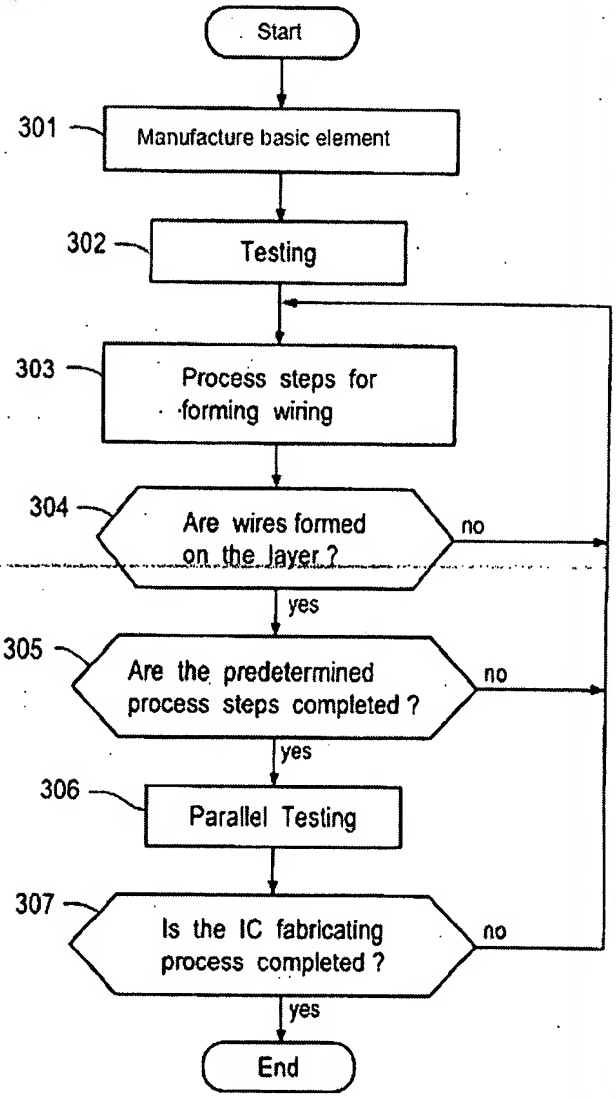

Start
301
Manufacture basic element
302
Testing
303
Process steps for forming wiring
304
Are wires formed on the layer ?
no
yes
305
Are the predetermined process steps completed ?
no
yes
306
Parallel Testing
307
Is the IC fabricating process completed ?
no
yes
End

Figure 20

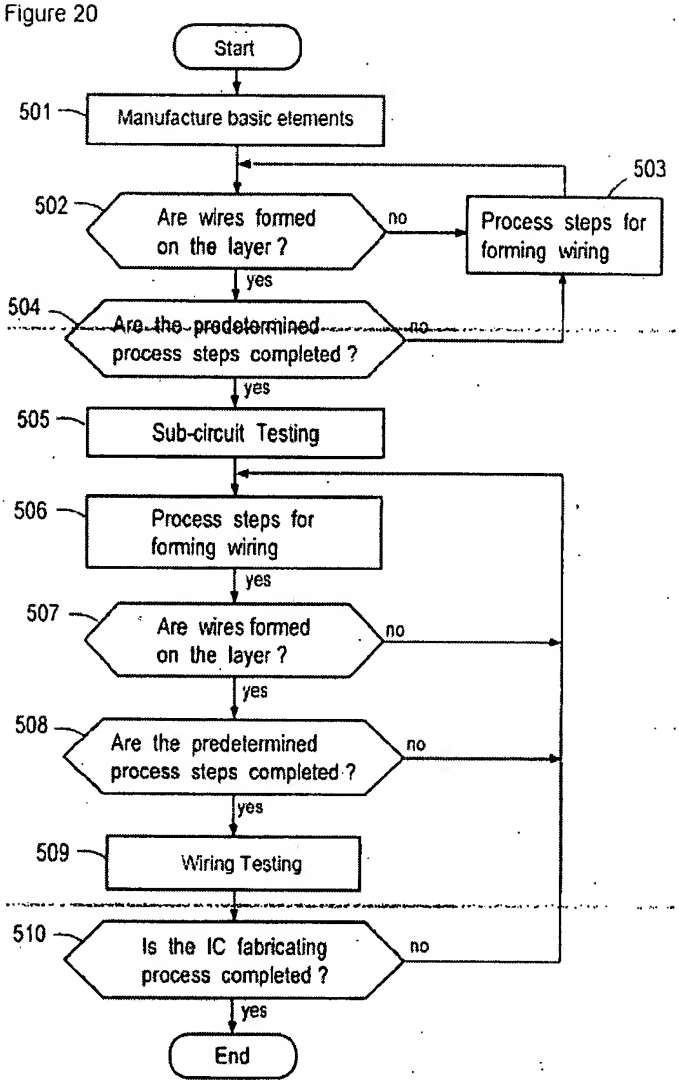

Start
501
Manufacture basic elements
503
502
Are wires formed on the layer ?
no
Process steps for forming wiring
yes
504
Are the predetermined process steps completed ?
no
yes
505
Sub-circuit Testing
506
Process steps for forming wiring
yes
507
Are wires formed on the layer ?
no
yes
508
Are the predetermined process steps completed ?
no
yes
509
Wiring Testing
510
Is the IC fabricating process completed ?
no
yes
End

Figure 21

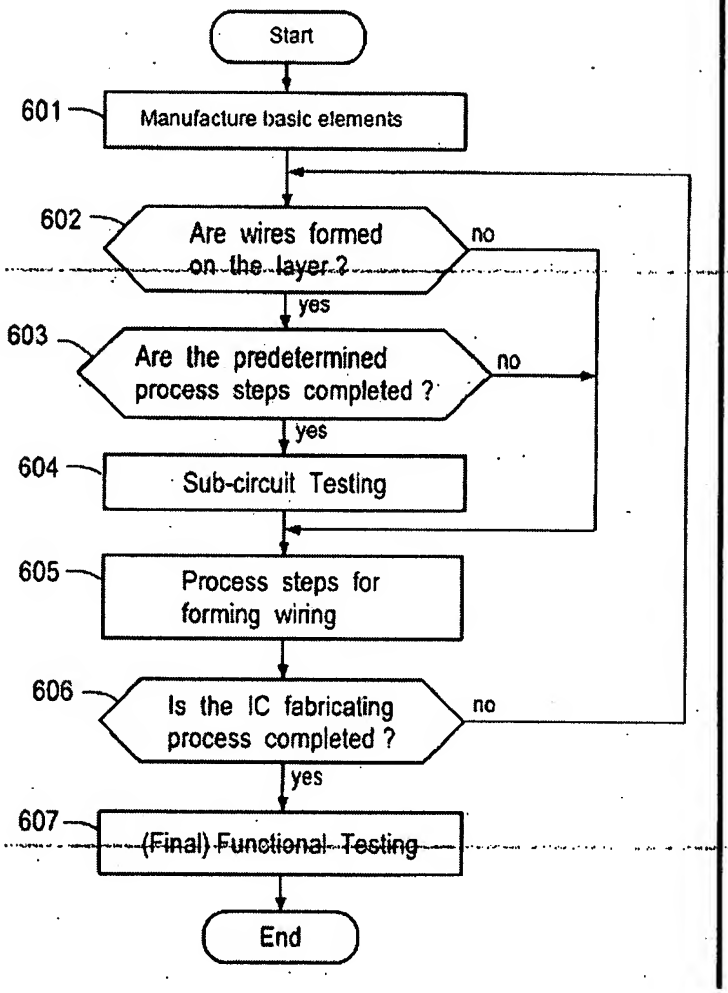
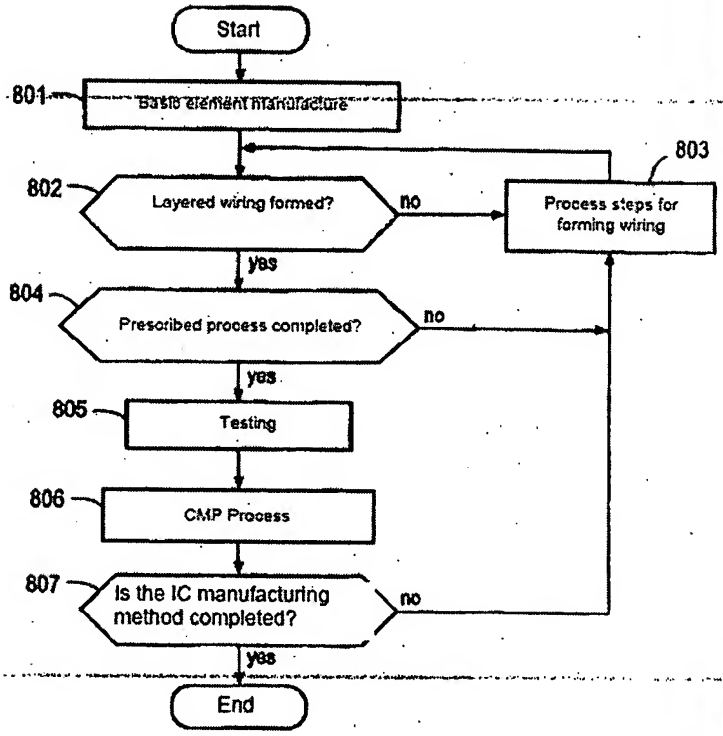

Start
601
Manufacture basic elements
602
Are wires formed on the layer ?
no
yes
603
Are the predetermined process steps completed ?
no
yes
604
Sub-circuit Testing
605
Process steps for forming wiring
606
Is the IC fabricating process completed ?
no
yes
607
(Final) Functional Testing
End

Figure 22


Start
801
Basic element manufacture
803
802
Layered wiring formed?
no
Process steps for forming wiring
yes
804
Prescribed process completed?
no
yes
805
Testing
806
CMP Process
807
Is the IC manufacturing method completed?
no
yes
End